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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,586	11/05/2001	Russell Francis	00CT18153314	2454

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,586	FRANCIS ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,13,15,16,18-21,23,25-32,34,35 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,13,15,16,18-21,23,25-32,34,35 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated November 8, 2004.

2. Claims 12-13, 15-16, 18-21, 23, 25-32, 34-35, and 37 are presented for examination. Applicant has canceled claims 1-11, 14, 17, 22, 24, 33, and 36.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12, 13, 15, 16, 18-21, 23, 25-32, 34, 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, US Patent 5677849, in view of Matoba, US Patent 5913068.

5. In re claim 12, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries], each responsive to a respective local clock signal [clock signals 40-43] [col.2, ll.42-53; col.5, ll.65-66].
- At least one system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals [col.3, l.63 -- col.4, l.34].

- A power control manager [central arbiter 1] connected to said circuit blocks via respective clock enable lines [start_clock lines 15-18] for selectively providing a shutdown signal [start_clock 15-18] thereto [fig.1; col.2, l.53 – col.3, l.12; start_clock is set high to shut down].
- Each circuit block comprising a local power control circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received [col.3, ll.5-12, ll.21-47; col.4, ll.35-53; kill_clock is low when circuit block is active].

6. Smith did not discuss details of a register.

7. Matoba discloses a system comprising:

- A power control manager [system controller 15] comprising at least one register [16a] connected to respective clock enable lines [intr 0-3] for storing data indicating logic states of the shutdown signals [col.8, ll.3-11, ll.48-53].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Matoba before him at the time the invention was made, to modify the SOC taught by Smith to include the register and CPU taught by Matoba, in order to obtain the SOC comprising a power control manager comprising at least one register for storing data indicating logic states of the shutdown signals and a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said at least one register. One of ordinary skill in the art would have been motivated to make such a

combination as it provides a way for controlling power consumption amongst multiple functional blocks through various detecting means [Matoba: col.1, l.60 -- col.2, l.52].

9. As to claims 13 and 21, Smith discloses that each local power control circuit comprises a clock separation circuit [NAND 44-47] connected to the power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

10. As to claim 15, Smith discloses that each circuit block further comprises a block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed to perform a function] having a status line [kill_clock lines 19-22] connected to said local power control circuit for providing a status signal thereto indicating whether said circuit block is in the active or idle state [fig.1; col.3, ll.5-12; col.4, ll.35-53].

11. As to claims 16 and 23, Smith discloses the local power control circuit that comprises a logic circuit [NAND 44-47, flip flops 23-26, inverters 36-39] having a first input [NAND 44-47] connected to the respective power down request line, a second input [NAND-44-47] connected to the respective status line, and a third input [flip flops 23-26] connected to the system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal [fig.1; col.3, ll.21-57; col.3, l.61 -- col.4, l.53].

12. As to claims 18 and 25, Matoba discloses a central processing unit [CPU #0] connected to the power control manager [15] for determining whether each circuit block [CPUs] is in the active or idle state by querying the at least one register [fig.1; col.8, ll.3-11].

13. As to claim 19, Smith discloses said at least one system clock that comprises a plurality of system clocks, each system clock for providing the system clock signal to selected circuit blocks [fig.1; clk_in 35 is branched off to multiple system clocks to inputs 31-34 and 27-30 of each block].

14. In re claim 20, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries].
- A system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto [col.3, l.63 -- col.4, l.34].
- A power control manager [central arbiter 1] connected to said circuit blocks for selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].
- Each circuit block comprising
- A block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed in order to provide the status signal] providing a status signal [kill_clock] indicating whether said circuit block is in an active or idle state [col.3, ll.21-47].
- A local power control circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the status signal indicates said circuit block is in the active state when the shutdown signal is received [col.3, ll.5-12, ll.21-47; col.4, ll.35-53; kill_clock is low when circuit block is active].

- Said power control manager being connected to each local power control circuit through a respective clock enable line [start_clock lines 15-18] for providing the shutdown signal [start_clock 15-18] thereto [fig.1; col.2, l.53 – col.3, l.12; start_clock is set high to shut down].

15. Smith did not discuss details of a register.

16. Matoba discloses a system comprising:

- A power control manager [system controller 15] comprising at least one register [16a] connected to respective clock enable lines [intr 0-3] for storing data indicating logic states of the shutdown signals [col.8, ll.3-11, ll.48-53].

17. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Matoba before him at the time the invention was made, to modify the SOC taught by Smith to include the register and CPU taught by Matoba, in order to obtain the SOC comprising a power control manager comprising at least one register for storing data indicating logic states of the shutdown signals and a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said at least one register. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for controlling power consumption amongst multiple functional blocks through various detecting means [Matoba: col.1, l.60 -- col.2, l.52].

18. In re claim 26, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries].

- A system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto [col.3, l.63 -- col.4, l.34].
- A power control manager [central arbiter 1] connected to said circuit blocks through a respective clock enable line [start_clock to NAND 44-47 which are part of respective circuit blocks] for selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].
- Each circuit block comprising a local power control circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the the circuit block is in the active state when the shutdown signal is received [col.3, ll.5-12, ll.21-47; col.4, ll.35-53; kill_clock is low when circuit block is active].

19. Smith did not discuss details of a register.

20. Matoba discloses a system comprising:

- A power control manager [system controller 15] that comprises at least one register [16a] connected to clock enable lines [intr 0-3] for storing data indicating logic states of the shutdown signals [col.8, ll.3-11, ll.48-53].
- A central processing unit [CPU #0] connected to the power control manager [fig.1] for determining whether each circuit block [CPUs] is in the active or idle state by querying the at least one register [col.8, ll.3-11].

21. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Matoba before him at the time the invention was made, to modify the SOC taught by Smith to include the register and CPU taught by Matoba, in order to obtain the SOC comprising

a power control manager comprising at least one register for storing data indicating logic states of the shutdown signals and a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said at least one register. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for controlling power consumption amongst multiple functional blocks through various detecting means [Matoba: col.1, l.60 -- col.2, l.52].

22. As to claim 27, Smith discloses that each local power control circuit comprises a clock separation circuit [NAND 44-47] connected to the power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

23. As to claim 28, Smith discloses that the power control manager is connected to each local power control circuit through a respective clock enable line [start_clock lines 15-18] for providing the shutdown signal thereto [fig.1; col.3, ll.5-12].

24. As to claim 29, Smith discloses that each circuit block further comprises a block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed to perform a function] having a status line [kill_clock lines 19-22] connected to said local power control circuit for providing a status signal thereto indicating whether said circuit block is in the active or idle state [fig.1; col.3, ll.5-12; col.4, ll.35-53].

25. As to claim 30, Smith discloses the local power control circuit that comprises a logic circuit [NAND 44-47, flip flops 23-26, inverters 36-39] having a first input [NAND 44-47] connected to the respective power down request line, a second input [NAND-44-47] connected to the respective status line, and a third input [flip flops 23-26] connected to the system clock,

and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal [fig.1; col.3, ll.21-57; col.3, l.61 -- col.4, l.53].

26. In re claims 31-32, 34-35, and 37, Smith and Matoba taught each and every limitation of the claim as discussed above in reference to claims 12-13, 15-16, and 18. Claims 31-32, 34-35, and 37 are directed to the SOC implementing the method of claims 12-13, 15-16, and 18. Smith and Matoba taught the SOC as set forth in claims 12-13, 15-16, and 18. Therefore, Smith and Matoba also taught the method as set forth in claims 31-32, 34-35, and 37.

Response to Arguments

27. All rejections of claim limitations as filed prior to Amendment dated November 8, 2004 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth.

28. Applicant's arguments, with respect to claim 12 [20, 26, and 31 are similar], have been fully considered but they are not persuasive.

29. Firstly, Applicant alleges that "there is no proper motivation to modify the Smith patent in the manner set forth by the Examiner... one of ordinary skill in the art would not look to modify the power control manager 1 as illustrated in fig.1 of Smith to include a register as disclosed in Matoba." In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir.

1992). In this case, Examiner specifically indicated the motivation of providing a way for controlling power consumption amongst multiple functional blocks through various detecting means to be found in col.1, l.60 – col.2, l.52 of Matoba.

30. Secondly, Applicant alleges that Smith "teaches away from using a register in the power control manager 1" and references various potions of Smith to *conclude* that "Smith thus fails to make any reference to the logic states of the respective clock enable signals being stored in the power control manger 1". Examiner notes that Applicant's allegation is a conclusion and not an indisputable fact that can be referenced in Smith. In fact, Applicant did not specifically point to anywhere in Smith that prohibited the use of a register in the power control manager 1.

31. Finally, Applicant alleges that "only in hindsight, and having the benefit of the Applicant's disclosure, would the skilled artisan possibly be motivated to modify the power control manger 1 in Smith to include a register as disclosed in Matoba." In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In the instant case, all knowledge including motivation can be found in Smith and Matoba as set forth in the rejections.

32. Therefore, as demonstrated above, Applicant's arguments, with respect to claim 12 [20, 26, and 31 are similar], are not persuasive and the rejections are hereby maintained.

33. All other claims were not argued separately and their respective rejections are thus maintained.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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Tse Chen
January 13, 2005